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| 10/828,547 | 04/19/2004 | Lukas P.P.P. van Ginneken | MDAI.001US3 | 3884 |

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| EXAMINER | |
|---|---|
| SIEK, VUTHE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

| NOTIFICATION DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,547 | VAN GINNEKEN, LUKAS P.P. | |
| | Examiner | Art Unit | |
| | Vuthe Siek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/828,547 and amendment filed on 9/19/2007. Claims 2-15 remain pending in the application.

### *Claim Objections*

2. Claims 5, 6, 9, 10 and 13 are objected to because of the following informalities: claims 5-6,"attempting" is not a definite claim language and need to be changed to a definite claim language; claims 6, "maintaining the delay values", need clarification as which delay values. In claim 9, "the theory of logical effort" lack antecedent basis; claim 10, "the preferred gain of the cells" lacks antecedent basis; claim 13, "the typical load of the cells" lack antecedent basis. Appropriate correction is required.

### *Double Patenting*

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 2-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-54 of U.S. Patent No. 6,453,446 B1. Although the conflicting claims are not identical, they are not patentably

distinct from each other because the claims in the instant application and patent are substantial similar. They are related to an automated method for designing an IC layout in order to meet timing constraints. The patent claims anticipate the claims in the instant application.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2-15 is rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (5,737,237).

7. As to claim 2, Tanaka et al. teach an automated method for designing an integrated circuit layout with a computer, comprising the steps of: (a) selecting a plurality of cells that are intended to be used in the integrated circuit layout (Fig. 1(a), which leaf cells are selected from leaf cell library; Fig. 10; 14(a-b); (b) determining initial delay values associated with the cells (Fig. 1(a) prior to determining an initial placement of the cells (Fig. 3; Fig. 14(a)) (delay constraints associated with the cells prior an initial placement of the cells ; and (c) performing an initial placement of the cells (Fig. 3, 8).

8. As to claim 3, Tanaka et al. teach determining an initial size or area of the cells in response to the initial placement of the initial delay values (Fig. 1(a) leaf cells stored in leaf cell library are prepared, initial size or area of the cells are determined; Fig. 3 describes calculation of objective function including delay calculation).

9. As to claim 4, Tanaka et al. adjusting the initial delay values of the cells if necessary to meet predetermined timing constraints (perform drive ability optimization, Fig. 1(a); Fig. 1(b) describes cell placement improvement process to meet delay constraints; Fig. 3 selection of placement to satisfy predetermined timing constraint or delay constraint).

10. As to claim 5, Tanaka et al. teach attempting to determine a size or area of the cells that will approximately maintain the adjusted delay values (Fig. 6(a) show an example of delay constraint along the line 163, where buffer 161 include transistors that can be sized to maintain the adjusted delay values or delay constraints).

11. As to claim 6, Tanaka et al. teach after determining the initial size or area of the cells, attempting to further adjust the size or area of the cells in order to approximately maintain the delay values (size or area of the cells are adjustable or sizeable to meet delay constraints or area constraints).

12. As to claim 7, Tanaka et al. teach routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells (generating a layout data, where the layout data is obtained from a finalized size or area of the selected plurality of cells from leaf cell library, Fig. 1a-b).

13. As to claim 8, Tanaka et al. teach wherein the initial delay values are determined using gain (cell placement improvement process describes in Fig. 1b must use gain).

14. As to claim 9, Tanaka et al. teach wherein the initial delay values are determined using the theory of logical effort (calculation of delays must use the theory of logical effort such as connection information).

15. As to claim 10, Tanaka et al. teach wherein the initial delay values are determined by finding the preferred gain of the cells (the improvement placement process finds the preferred gain of the cells in order to meet delay constraints).

16. As to claim 11, Tanaka et al. teach wherein the preferred gain of the cells is determined using a continuous buffering assumption (Fig. 6a-b).

17. As to claim 12, Tanaka et al. teach wherein the initial delay values are determined during library analysis (Fig. 1a, cells in leaf cell library are prepared).

18. As to claim 13, Tanaka et al. teach wherein the initial delay values are determined using the typical load of the cells (drive ability optimization process determines delay according to load of the cells, Fig. 6b shows loads driven by driving buffer 164; see Fig. 6a).

19. As to claim 14, Tanaka et al. teach wherein the typical load is determined based on gain considerations (drive ability optimization and cell placement improvement process are performed based on gain considerations in order to meet delay constraints or area constraints).

20. As to claim 15, wherein the size or area of the cells is variable and not fixed at the time the cells are selected (drive ability optimization process is performed on sizeable cells).

21. Claims 2-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Frankle et al. (5,521,837).

22. As to claim 2, Frankle et al. teach an automated method for designing an integrated circuit layout with a computer comprising the steps of: (a) selecting a plurality of cells that are intended to be used in the integrated circuit layout (Fig. 12 show cells that are intended to be used in the IC layout); (b) determining initial delay values associated with the cells prior to determining an initial placement of the cells (Fig. 10-11; Fig. 10 describes compute suggested delay limits and Fig. 11 describes compute initial delay; Fig. 14 describes compute initial delays) and (c) performing an initial placement of the cells (Fig. 10 describes the computed delays are supplied to an initial placement; col. 21 lines 35-37).

23. As to claim 3, Frankle et al. teach determining an initial size or area of the cells in response to the initial placement of the initial delay values (at least see col. 18, lines 40-62).

24. As to claim 4, Frankle et al. teach adjusting the initial delay values of the cells if necessary to meet predetermined timing constraints (at least see col. 18 lines 40-67; col. 19 lines 1-2).

25. As to claim 5, Frankle et al. teach attempting to determine a size or area of the cells that will approximately maintain the adjusted delay values (at least see col. 18 lines 40-67; col. 19 lines 1-2).

26. As to claim 6, Frankle et al. teach after determining the initial size or area of the cells, attempting to further adjust the size or area of the cells in order to approximately maintain the delay values (at least see col. 18 lines 40-67; col. 19 lines 1-2).

27. As to claim 7, Frankle et al. teach routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells (at least see col. 17 lines 59-67; col. 18 lines 1-67; col. 19 lines 1-2) .

28. As to claim 8, Frankle et al. teach wherein the initial delay values are determined using gain (at least see col. 15 lines 10-67; col. 16 lines 1-29).

29. As to claim 9, Frankle et al. teach wherein the initial delay values are determined using the theory of logical effort (at least see Fig. 10-12).

30. As to claim 10, Frankle et al. teach wherein the initial delay values are determined by finding the preferred gain of the cells (at least see Fig. 10-12).

31. As to claim 11, Frankle et al. teach wherein the preferred gain of the cells is determined using a continuous buffering assumption (at least see Fig. 10-12). Note that using a buffering assumption is known to practitioners and it is inherently within the art in order to improve delay to meet timing constraints.

32. As to claim 12, Frankle et al. teach wherein the initial delay values are determined during library analysis (Fig. 10-12). Each of the blocks or cells has internal

delays that can be modified or changed by varying its sizes and functions (at least see col. 13; col. 18, starting line 40).

33. As to claim 13, wherein the initial delay values are determined using the typical load of the cells (at least see col. 9 lines 14-63; summary; Fig. 12).

34. As to claim 14, wherein the typical load is determined based on gain considerations (at least see Fig. 10-12).

35. As to claim 15, wherein the size or area of the cells is variable and not fixed at the time the cells are selected (col. 18 lines 40-63).

36. Applicants are requested to consider in their entirety the cited references used in the rejection.

37. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Vuthe Siek
Primary Examiner, A.U. 2825